IN THE CLAIMS:

Kindly amend claims 1-2 and add new claims 3-15 as shown in the following listing of claims, which replaces all previous versions and listings of claims in this application.

1. (currently amended) A semiconductor memory device comprising:

an external terminal receptive of a voltage ~~to which a voltage~~ for switching an operation mode ~~is applied~~;

a protective transistor connected between the external terminal and a ground, the protective transistor having a drain region and a gate electrode surrounding the drain region; and

a voltage detection circuit for detecting a voltage of the external terminal and outputting a switching signal for switching a first operation mode to a second operation mode when a value of the detected voltage is equal to or higher than a preselected voltage value. ~~is a predetermined voltage or higher,~~

~~wherein the protective transistor has a drain region surrounded by a gate electrode.~~

2. (currently amended) A semiconductor memory device according to ~~claim 1, wherein~~ claim 1; wherein the voltage detection circuit has a plurality of MOS transistors connected in series between the external terminal and the ground, one of

the MOS transistors having a high breakdown voltage; and wherein the voltage detection circuit ~~and~~ outputs the switching signal from a node in the serially connected ~~among the~~ MOS transistors. ~~connected in series,~~

~~wherein a MOS transistor of the plurality of MOS transistors connected to the external terminal is a high breakdown voltage MOS transistor.~~

3. (new) A semiconductor memory device according to claim 1; wherein the voltage detection circuit has a first NMOS transistor having a drain connected to the protective transistor, a first PMOS transistor connected to a source of the first NMOS transistor, a second PMOS transistor connected to a drain of the first PMOS transistor, and a second NMOS transistor connected to a drain of the second PMOS transistor.

4. (new) A semiconductor memory device according to claim 3; wherein the first NMOS transistor has a high breakdown voltage.

5. (new) A semiconductor memory device according to claim 4; wherein the protective transistor comprises a MOS transistor having a low breakdown voltage.

6. (new) A semiconductor memory device comprising:

an external terminal receptive of a voltage for switching between first and second operation modes of the semiconductor memory device;

a protective transistor connected directly to the external terminal and having a drain region and a gate electrode surrounding the drain region for suppressing a terminal leak current in at least one of the first and second operation modes; and

a voltage detection circuit for detecting a voltage of the external terminal and outputting a switching signal for switching from the first operation mode to the second operation mode.

7. (new) A semiconductor memory device according to claim 6; wherein the voltage detection circuit has a plurality of MOS transistors connected in series between the external terminal and a ground, one of the MOS transistors having a high breakdown voltage; and wherein the voltage detection circuit outputs the switching signal from a node in the serially connected MOS transistors.

8. (new) A semiconductor memory device according to claim 6; wherein the voltage detection circuit has a first NMOS transistor having a drain connected to the protective transistor, a first PMOS transistor connected to a source of the first NMOS transistor, a second PMOS transistor connected to a drain of the first PMOS transistor, and a second NMOS transistor connected to a drain of the second PMOS transistor.

9. (new) A semiconductor memory device according to claim 8; wherein the first NMOS transistor has a high breakdown voltage.

10. (new) A semiconductor memory device according to claim 9; wherein the protective transistor comprises a MOS transistor having a low breakdown voltage.

11. (new) A semiconductor memory device comprising:

an external terminal receptive of a voltage for switching an operation mode;

a protective transistor connected between the external terminal and a ground, the protective transistor having a drain region and a gate electrode disposed in overlapping relation with an end of the drain region; and

a voltage detection circuit for detecting a voltage of the external terminal and outputting a switching signal for switching a first operation mode to a second operation mode when a value of the detected voltage is equal to or higher than a preselected voltage value.

12. (new) A semiconductor memory device according to claim 11; wherein the voltage detection circuit has a plurality of MOS transistors connected in series between the external terminal and a ground, one of the MOS transistors having a high breakdown voltage; and wherein the voltage detection circuit outputs the switching signal from a node in the serially connected MOS transistors.

13. (new) A semiconductor memory device according to claim 11; wherein the voltage detection circuit has a first NMOS transistor having a drain connected to the protective transistor, a first PMOS transistor connected to a source of the first NMOS transistor, a second PMOS transistor connected to a drain of the first PMOS transistor, and a second NMOS transistor connected to a drain of the second PMOS transistor.

14. (new) A semiconductor memory device according to claim 13; wherein the first NMOS transistor has a high breakdown voltage.

15. (new) A semiconductor memory device according to claim 14; wherein the protective transistor comprises a MOS transistor having a low breakdown voltage.